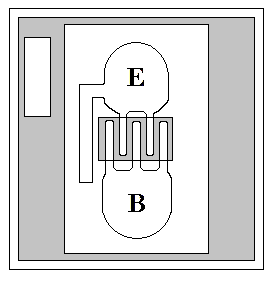
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**.015”**

**.015”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .003” min.**

**Backside Potential: Collector**

**Mask Ref: DLA**

**APPROVED BY: DK DIE SIZE .015” X .015” DATE: 11/10/21**

**MFG: SPRAGUE / ALLEGRO THICKNESS .006” P/N: 2N918**

**DG 10.1.2**

#### Rev B, 7/19/02